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Reducing the power consumption of level-crossing analog-to-digital converters by using a signal activity monitoring circuit

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ABSTRACT

An activity monitoring circuit is proposed for reducing the activity and thus the power consumption of the synchronous level-crossing analog-to-digital converter. The proposed technique does not affect the output samples, the average sampling frequency, or the accuracy. Utilizing a floating-window structure, high accuracy is achieved while the suggested activity monitoring technique significantly reduces power consumption to levels comparable to the fixed-window structure. To show the effectiveness of the proposed structure, two converters are designed for ECG and neural signal acquisition in a 0.18 μm CMOS process. For ECG (Neural), the power consumption and the activity of the converter are decreased by 42.3 % (38.41 %) and 45.4 % (44.5 %), respectively. Post-layout simulation results show a power consumption of 26.8 nW and an effective number of bits (ENOB) of 9 bits for ECG application. The power consumption is 223.3 nW and the ENOB is 6 bits for neural application. This makes the proposed structure suitable for ultra-low power wearable and implantable biopotential-recording applications.

1. Introduction

Decreasing power consumption is the main challenge of the battery-powered devices such as sensor networks, smart tags, and wearable or implantable medical devices [1]. In these applications, most of the power is usually consumed in the communication blocks, the power consumption of which is directly proportional to the data transfer rate. Data transfer rate is related to the sampling rate and the resolution provided by the analog-to-digital converter (ADC). In most of these applications, the signals are slow and sparse. Therefore, instead of using a constant sampling rate which is determined based on the highest frequency component of the input signal and may result in a significant waste of power in inactive low-frequency intervals, the sampling frequency can be dictated by the input signal using event-driven sampling schemes [1,2].

Among the various event-driven sampling schemes, level-crossing sampling (LC-sampling) is an attractive one in which the sampling rate is proportional to the variation speed of the input signal and no sample is taken from the inactive parts. It is shown that using LC-sampling can result in lower activity and power consumption in many applications such as audio, ECG, and neural signal recording [3–5].

Although several structures have been proposed for implementing the level-crossing analog-to-digital converters (LCADCs) for different design aspects [6], there is still a long way to reach the optimum structure in most applications. Most ultra-low power structures, which are mainly based on the fixed-window mechanism, do not have high accuracies [2,5,7,8]. There are more accurate structures based on the floating-window mechanism, but the power consumption of them appears to be more than their fixed-window counterparts in similar applications [1,9–11]. Although the main benefit of using LC-sampling is the considerable power reduction in the following transceiver and processor, additional efforts are required to improve the LCADC structures to achieve a more accurate and power-efficient system.

In this work, an activity monitoring circuit is proposed in order to reduce the power consumption of floating-window LCADCs while preserving their high accuracy. The proposed circuit reduces the activity of the LCADCs with synchronous implementation by changing the frequency of the operating clock based on the input signal activity. Also, a modified structure of the converter is utilized with a single comparator and one reference voltage rather than two, using which the occupied silicon area is reduced considerably.

The paper is organized as follows. The conventional structures of

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